CLAIMS

1. A method for generating a switching vector comprising:

providing a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and an internal node, wherein the internal node is at least one of a node located within a feedback path of the circuit and a node capable of assuming a first state, a second state, and a third state;

generating a Boolean transition function which represents the side states of the side inputs that cause the predetermined output transition to occur; and

determining the switching vector which satisfies the Boolean transition function.

2. The method of claim 1, wherein generating the Boolean transition function comprises:

generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition;

selecting a first term within one of the before transition function or the after transition function, wherein the first term is expressed as a function of the internal node;

expanding the first term with respect to the internal node to obtain an expansion equation; and

using the expansion equation to generate the Boolean transition function.

3. The method of claim 2, wherein generating the Boolean transition function further comprises substituting the first term with the expansion equation.

4. The method of claim 3, wherein the expansion equation defines a reduction value for the internal node.

5. The method of claim 4, wherein generating the Boolean transition function further comprises:

selecting a second term within one of the before transition function or the after transition function, wherein the second term is expressed as a function of the internal node; and

substituting the reduction value for the internal node in the second term.

6. The method of claim 3, wherein the internal node is capable of assuming the first state, the second state, and the third state, the third state being a different state from the first state and the second state and wherein the expansion equation comprises:

a first term corresponding to the internal node assuming the first state;

a second term corresponding to the internal node assuming the second state; and

a third term corresponding to the internal node assuming the third state.

7. The method of claim 6, wherein the first state comprises logic high state, the second state comprises a logic low state, and the third state comprises at least one of an unknown state, a high impedance state, and a short circuit state.

8. The method of claim 3, wherein the circuit includes a second internal node, wherein the second internal node is at least one of a node located within a feedback path of the circuit and a node capable of assuming a first state, a second state, and a third state, and wherein generating the Boolean transition function further comprises:

selecting a second term within one of the before transition function or the after transition function, wherein the first term is expressed as a function of the second internal node;

expanding the second term with respect to the second internal node to obtain an expansion equation; and

substituting the second term with the expansion equation.

9. The method of claim 3, wherein when the expansion equation is satisfied, the first term is satisfied.

10. The method of claim 2, wherein the output and the internal node is a same node.

11. The method of claim 2, wherein the internal node is located within the feedback path of the circuit.

12. The method of claim 2, wherein the internal node is capable of assuming the first state, the second state, and the third state.

13. The method of claim 2, wherein the internal node is located within the feedback path of the circuit and is capable of assuming the first state, the second state, and the third state.

14. A method for generating a set of switching vectors comprising:

providing a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and a plurality of internal nodes, wherein each of the plurality of internal nodes is at least one of a node located within a feedback path of the circuit and a node capable of assuming a first state, a second state, and a third state; and

determining the set of switching vectors corresponding to the side states which results in the predetermined output transition, wherein the set of switching vectors is a subset of a full enumeration of all side states for the circuit.

15. The method of claim 14, where the set of switching vectors include only those switching vectors that result in the predetermined output transition.

16. The method of claim 14, wherein determining the set of switching vectors comprises:

generating a transition function corresponding to the predetermined input transition and predetermined output transition;

selecting a first term within the transition function, wherein the first term is expressed as a function of at least one internal node of the plurality of internal nodes;

expanding the first term with respect to the at least one internal node to obtain an expansion equation; and

using the expansion equation to reduce the transition function with respect to the at least one internal node to obtain a reduced transition function.

17. The method of claim 16, wherein the reduced transition function is not expressed as a function of any of the plurality of internal nodes.

18. The method of claim 16, wherein the set of switching vectors satisfies the reduced transition function.

19. The method of claim 16, wherein the expansion equation defines a reduction value for the at least one internal node, the method further comprising:

selecting a second term within the transition function, wherein the second term is expressed as a function of the at least one internal node; and

substituting the reduction value for the at least one internal node in the second term.

20. The method of claim 16, wherein the at least one internal node is capable of assuming the first state, the second state, and the third state, each of the first, second, and third state being a different state, and wherein the expansion equation comprises:

a first term corresponding to the at least one internal node assuming the first state;

a second term corresponding to the at least one internal node assuming the second state; and

a third term corresponding to the at least one internal node assuming the third state.

21. The method of claim 20, wherein the first state comprises logic high state, the second state comprises a logic low state, and the third state comprises at least one of an unknown state, a high impedance state, and a short circuit state.

22. A switching vector generator stored via at least one computer readable medium, the switching vector generator comprising:

a first set of instructions for receiving a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and an internal node, wherein the internal node is at least one of a node located within a feedback path of the circuit and a node capable of assuming a first state, a second state, and a third state;

a second set of instructions for generating a Boolean transition function which represents the side states of the side inputs that cause the predetermined output transition to occur; and

a third set of instructions for determining the switching vector which satisfies the Boolean transition function.

23. The switching vector generator of claim 22, further comprising:

a fourth set of instructions for generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition;

a fifth set of instructions for selecting a first term within one of the before transition function or the after transition function, wherein the first term is expressed as a function of the internal node;

a sixth set of instructions for expanding the first term with respect to the internal node to obtain an expansion equation; and

a seventh set of instructions for using the expansion equation to generate the Boolean transition function.

24. The switching vector generator of claim 23, further comprising an eighth set of instructions for substituting the first term with the expansion equation.

25. The switching vector generator of claim 24, wherein the expansion equation defines a reduction value for the internal node.

26. The switching vector generator of claim 25, further comprising:

a ninth set of instructions for selecting a second term within one of the before transition function or the after transition function, wherein the second term is expressed as a function of the internal node; and

a tenth set of instructions for substituting the reduction value for the internal node in the second term.

27. The switching vector generator of claim 24, wherein the internal node is capable of assuming the first state, the second state, and the third state, the third state being a different state from the first state and the second state and wherein the expansion equation comprises:

a first term corresponding to the internal node assuming the first state;

a second term corresponding to the internal node assuming the second state; and

a third term corresponding to the internal node assuming the third state.

28. The switching vector generator of claim 27, wherein the first state comprises logic high state, the second state comprises a logic low state, and the third state comprises at least one of an unknown state, a high impedance state, and a short circuit state.

29. A switching vector generator stored via at least one computer readable medium, the switching vector generator comprising:

a first set of instructions for receiving a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition

and the side states, and a plurality of internal nodes, wherein each of the plurality of internal nodes is at least one of a node located within a feedback path of the circuit and a node capable of assuming a first state, a second state, and a third state; and

a second set of instructions for determining the set of switching vectors corresponding to the side states which results in the predetermined output transition, wherein the set of switching vectors is a subset of a full enumeration of all side states for the circuit.

30. The switching vector generator of claim 29, further comprising:

a third set of instructions for generating a transition function corresponding to the predetermined input transition and predetermined output transition;

a fourth set of instructions for selecting a first term within the transition function, wherein the first term is expressed as a function of at least one internal node of the plurality of internal nodes;

a fifth set of instructions for expanding the first term with respect to the at least one internal node to obtain an expansion equation; and

a sixth set of instructions for using the expansion equation to reduce the transition function with respect to the at least one internal node to obtain a reduced transition function.

31. The switching vector generator of claim 30, wherein the expansion equation defines a reduction value for the at least one internal node, the switching vector generator further comprising:

a seventh set of instructions for selecting a second term within the transition function, wherein the second term is expressed as a function of the at least one internal node; and

an eighth set of instructions for substituting the reduction value for the at least one internal node in the second term.

32. The switching vector generator of claim 30, wherein the internal node is capable of assuming the first state, the second state, and the third state, each of the first, second, and third state being a different state, and wherein the expansion equation comprises:

a first term corresponding to the at least one internal node assuming the first state;

a second term corresponding to the at least one internal node assuming the second state; and

a third term corresponding to the at least one internal node assuming the third state.

33. The switching vector generator of claim 32, wherein the first state comprises logic high state, the second state comprises a logic low state, and the third state comprises at least one of an unknown state, a high impedance state, and a short circuit state.